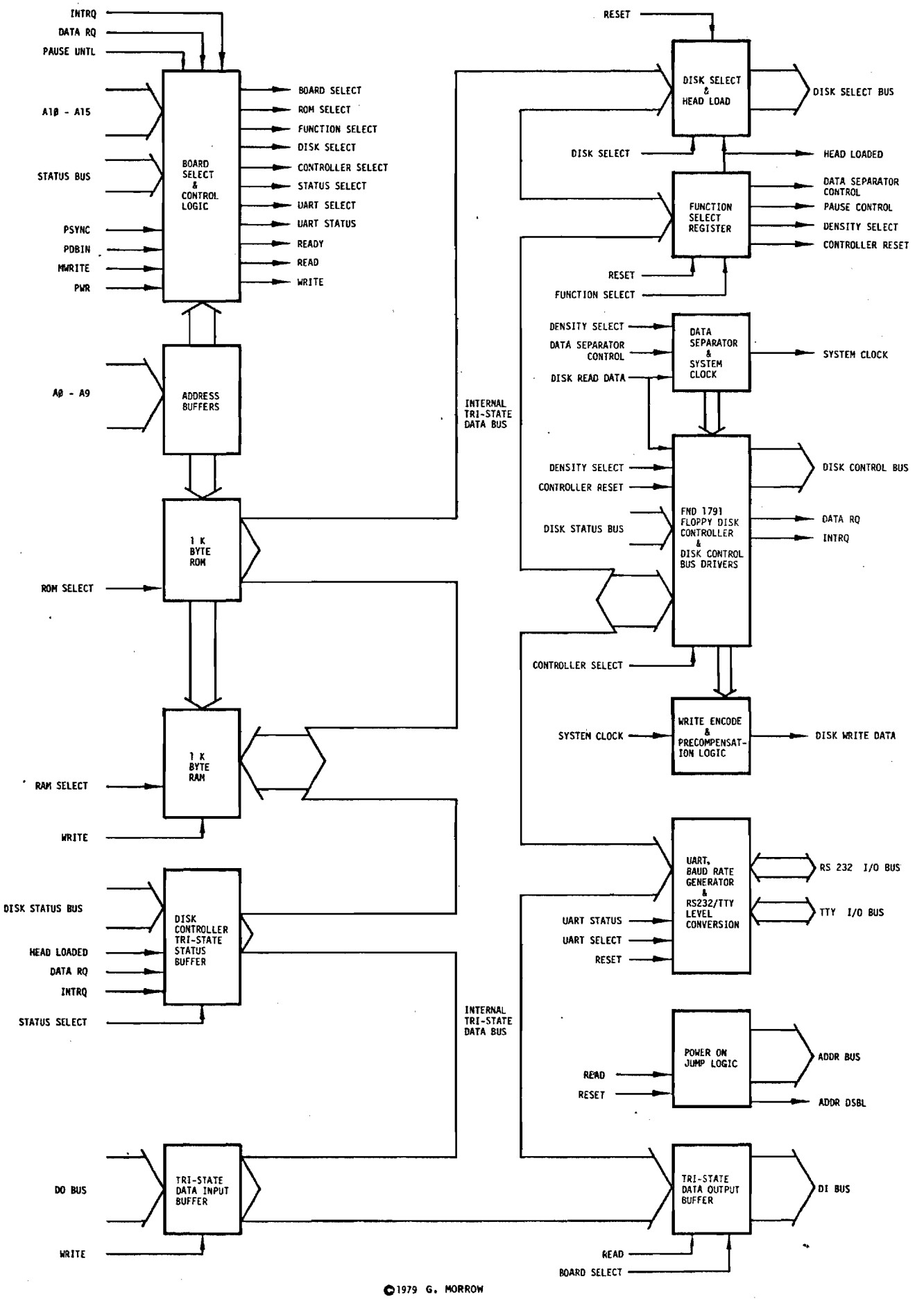
BLOCK DIAGRAM



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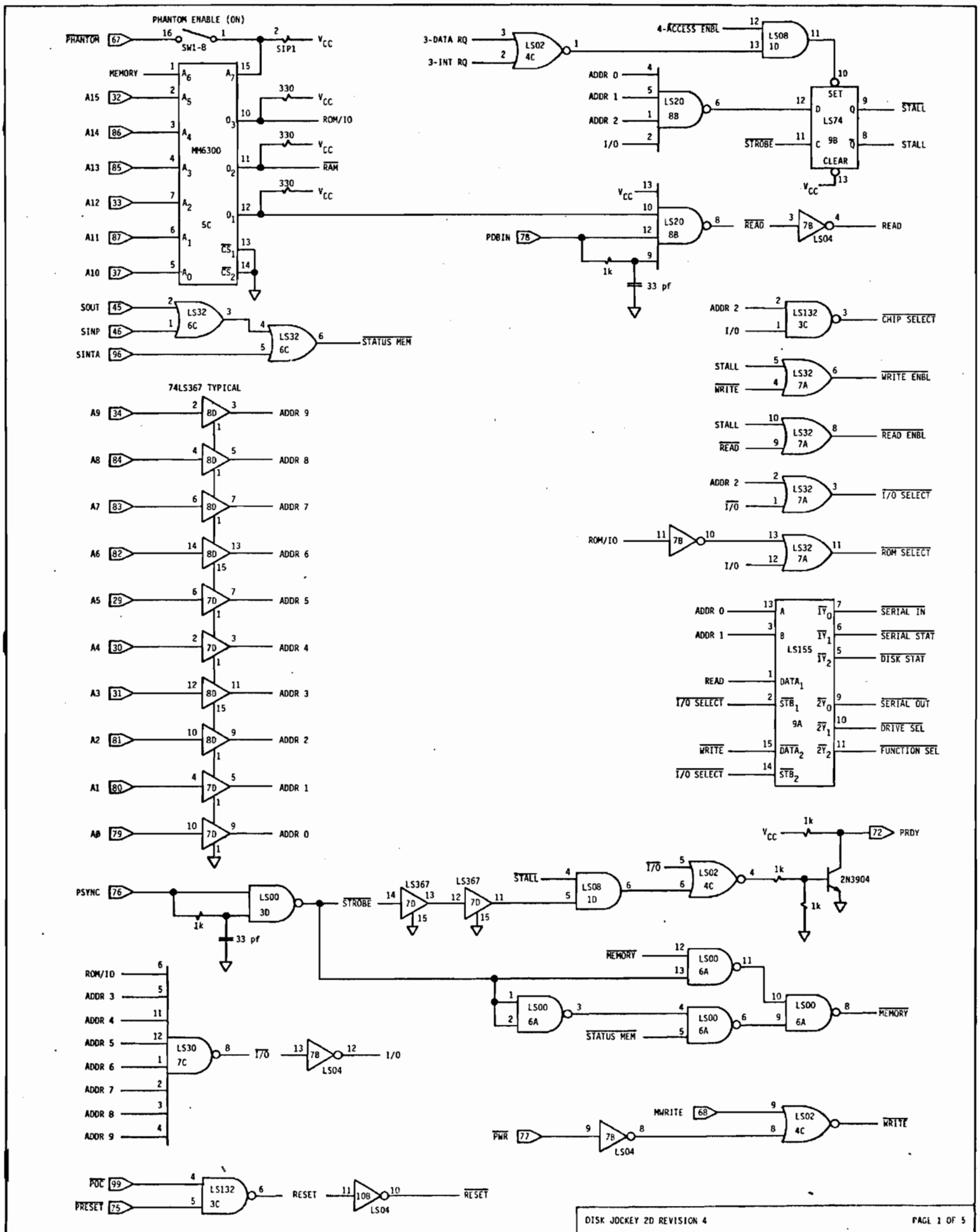

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BOARD SELECT LOGIC,ADDRESS BUFFERS

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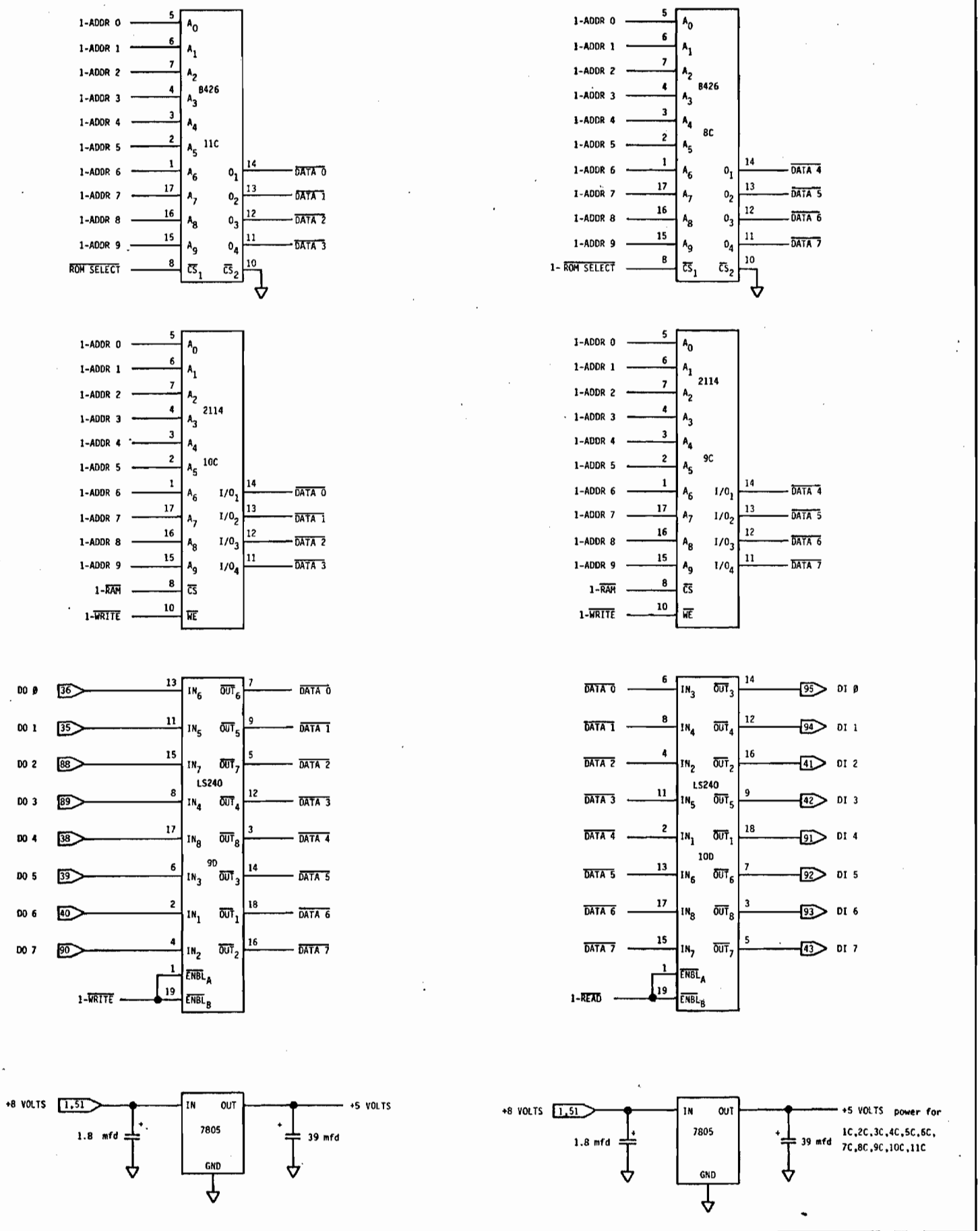

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RAM, ROM, AND DATA BUFFERS

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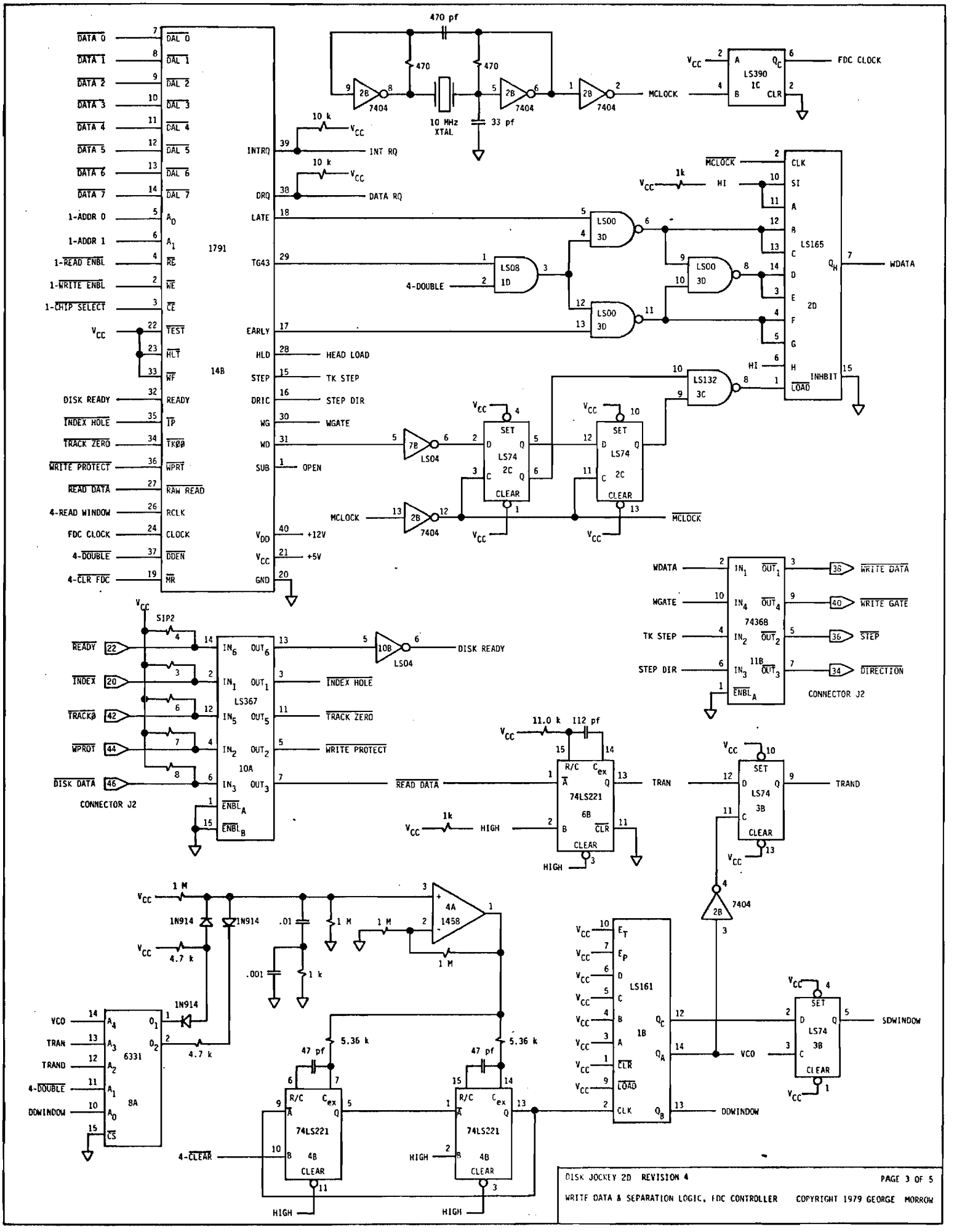

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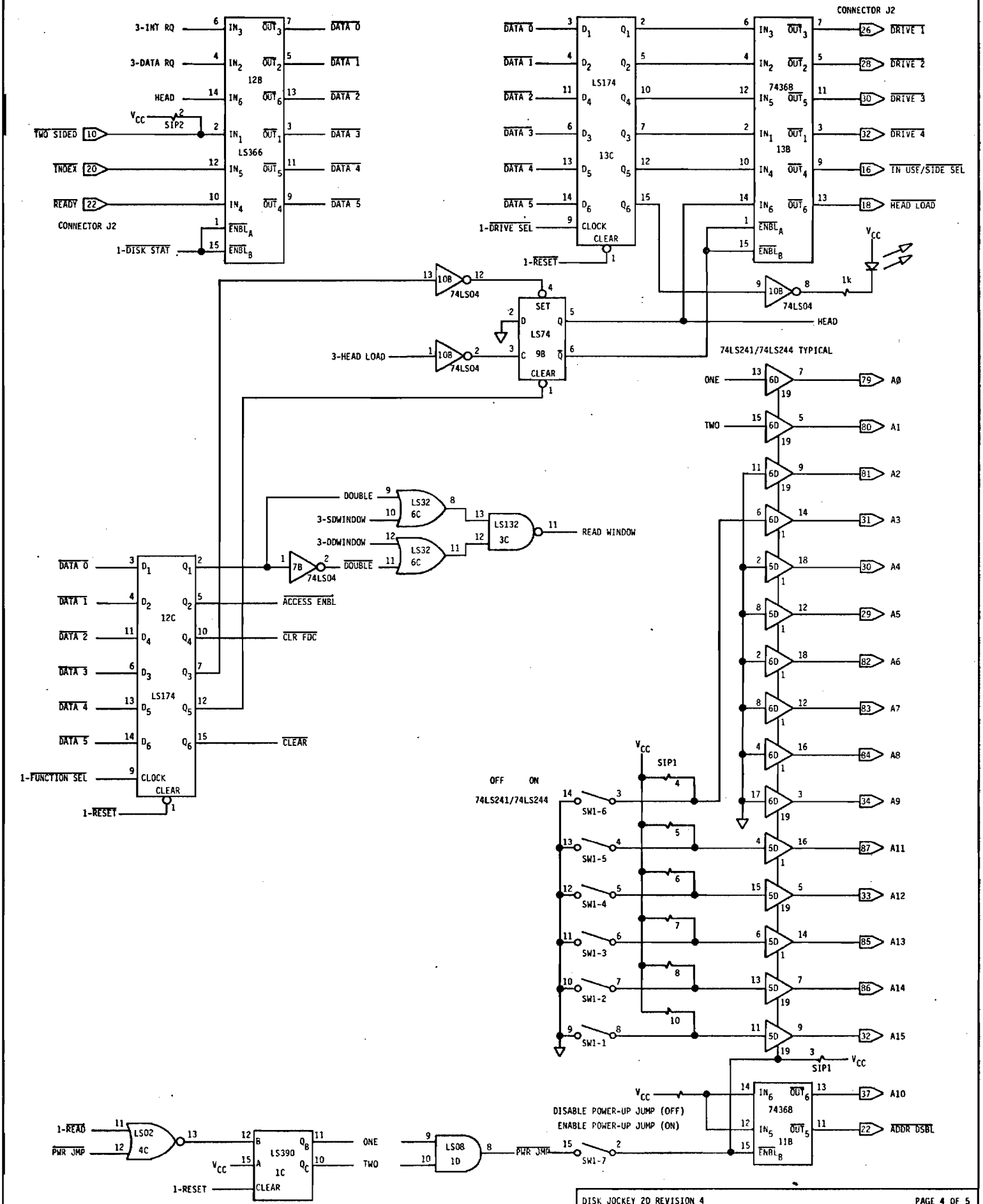
WRITE DATA & SEPARATION LOGIC, FDC CONTROLLER COPYRIGHT 1979 GEORGE MORROW


3-INT RQ
3-DATA RQ
HEAD
TWO SIDED
INDEX
READY
CONNECTOR J2
1-DISK STAT
12B
LS366
SIP2
DATA 0
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
LS174
13C
CLOCK
CLEAR
1-DRIVE SEL
1-RESET
CONNECTOR J2
74368
13B
DRIVE 1
DRIVE 2
DRIVE 3
DRIVE 4
IN USE/SIDE SEL
HEAD LOAD
1k
74LS04
SET
LS74
9B
HEAD
3-HEAD LOAD
74LS241/74LS244 TYPICAL
ONE
TWO
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A11
A12
A13
A14
A15
DOUBLE
3-SDWINDOW
3-DDWINDOW
LS32
6C
LS132
3C
READ WINDOW
7B
ACCESS ENBL
CLR FDC
12C
1-FUNCTION SEL
OFF ON
74LS241/74LS244
SW1-6
SW1-5
SW1-4
SW1-3
SW1-2
SW1-1
SIP1
DISABLE POWER-UP JUMP (OFF)
ENABLE POWER-UP JUMP (ON)
SW1-7
A10
ADDR DSBL
1-READ
PWR JMP
LS02
4C
LS390
1C
LS08
1D
DISK JOCKEY 2D REVISION 4
PAGE 4 OF 5
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FUNCTION REGISTER,DRIVE SELECT & POWER-UP JUMP LOGIC
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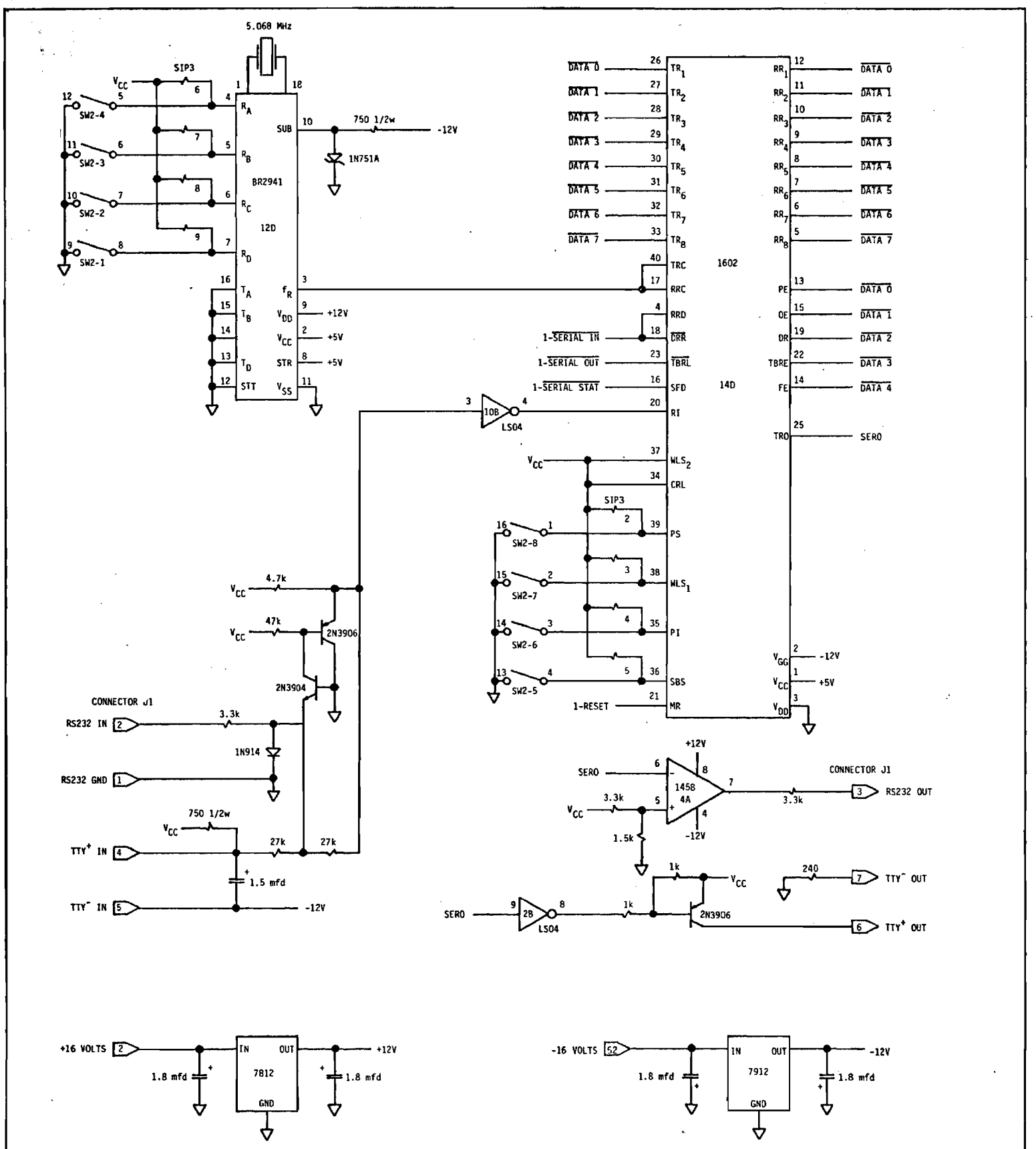

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SERIAL INTERFACE LOGIC

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