OPERATIONS
MANUAL

VERSAFLOPPY II

FLOPPY DISK CONTROLLER

JULY 1979

REVISION C
JULY, 1980

LIMITED WARRANTY

All SD Systems products assembled by SD personnel and functionally tested at our facility are warranted for a period of ninety (90) days from date of purchase to be free from defects of material and workmanship. Kits or other products functionally unfinished or semi-finished at the time of shipment from our facility are warranted for the same period in regard to material defects only, with no warranty, expressed or implied, covering workmanship of others. Should an SD Systems product fail to perform to specifications, obtain a Returned Material Authorization number from your dealer or from SD Systems. Include this number in all correspondence and with the returned product. Ship the item prepaid to SD Systems and it will, at our option, be repaired or replaced free of charge, provided the unit is received during the warranty period. Testing or repair work performed upon returned kits or other products assembled wholly or partially by others will be subject to a $35.00 minimum service charge unless such products are found to be non-functional due to defects in material purchased from SD Systems.

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Differences from Rev B to Rev C manual
Versafloppy II
Herb Johnson June 2013

Rev B references the FD1791B-1 FDC chip.
Rev C references the FD1795B FDC chip.

Rev B page 13, 3-7 Format Routine

NOTE: the 1791 requires different data in the gaps than the 1771 and therefore may not be able to read disks formatted on the SD-100 machines. In addition, the DDBIOS software uses the side byte on the diskette to determine if the diskette is single or double sided. Because of this, diskettes formatted on the SD-100 as double sided may appear as single sided on the SD-200. See FORMAT in SDOS Operating System manual for further information.

Rev C page 13, 3-7 Format Routine

Note 1: the DDBIOS software uses the side byte on the diskette to determine if the diskette is single or double sided. It thereform may misread disks formatted on an SD-100 as single-sided.

NOte 2: early boards used a 1791B-1 controller chip, which is not able to read disks formattted with all zeroes in the gaps between sectors. therefore, VF II boards with the 1791-B cannot read disks formatted by machnes with a 1771 controller chip (like the SD Systems SD-100).

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rev B page 16 - IC install list

R. U31 74LS273
S. U10 FD1791-B
T. U2   DUU-4-2400 Delay line
U. U1   16MHz oscillator
V. U3   LM 301AN

rev C page 16 - IC install list

R. U31 74LS273
S. U10 FD1795B
T. U3   LM 301AN

4. install U2   DUU-4-2400 Delay line
5. install U1   16MHz oscillator

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32 - 22 7030045 1MF capacitor C4 to C13, etc.

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32 - 21 7030007 .1MF capacitor C4 to C13, etc.

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SECTION I

GENERAL INFORMATION

1-1 INTRODUCTION

VERSAFLOPPY II™ is the new floppy controller board from SD SYSTEMS. It features the Western Digital FD1795 double density controller The unique feature of this board is that it may be used with mini or full-size floppy drives, single or double density, single or double sided, in any variation thereof. For example, a mini drive operating single density and a full-size drive operating double density may be utilized at the same time and information may be transferred from one to the other.

VERSAFLOPPY II was designed to be used optimally with SD SYSTEMS' SBC-200, single board computer, and Expandoram boards to form a complete, low cost, disk based computer. The VERSAFLOPPY II is designed for operation with the Z80 CPU and is not recommended for operation with other processors.

1-2 GENERAL DESCRIPTION

At the heart of the VERSAFLOPPY II is the powerful Western Digital FD1795B NMOS LSI double density controller chip. This device performs most of the timing and control functions required by floppy disk drives such as:

1. Head load/unload
2. Track seeking with verification
3. Address mark detection/generation
4. Serial to parallel data conversion during reads
5. Parallel to serial data conversion during writes
6. CRC error code checking/generation
7. IBM 3740 Soft Sector compatible reading
8. Signals for double density recording and precompensation

During sector reading and writing, the data rate is synchronized with the CPU by inserting wait states until the FD1795B is ready for the next word.
The VERSAFLOPPY II employs a phase locked loop in the data recovery circuit which insures a valid readback during double density operation.

1-3 SOFTWARE CONSIDERATIONS

The control function has been designed to be evenly distributed between the hardware circuit and the control software allowing a great deal of flexibility for the user. A version of the control software is supplied with the VERSAFLOPPY II in listing form configured to run on the SBC-100/200 single board computer. This may be modified to meet the user's specific software interface requirements, such as register usage, parameter hand-offs and data formats.

Also available from SD SYSTEMS is a version of SDOS configured to run on the SBC-100/200, VERSAFLOPPY II and 32K Expandoram II board combination. This allows using several disk based versions of high level languages.

SECTION II

FUNCTIONAL DESCRIPTION

2-1 INTRODUCTION

Functionally, the VERSAFLOPPY II consists of two main parts: hardware, and the software which controls it. The hardware allows the computer to control the drive selection, head loading, track seeks, formatting, reading and writing operations. The software, as described in Section 3, must direct the hardware in each of these operations. The major functions contained in the VERSAFLOPPY II hardware are shown in the block diagram. (Fig. 2-1) Table 2-1 lists the S-100 Bus signals used by the VERSAFLOPPY II.

2-2 FD1791B-1

The FD1797, the floppy disk controller chip, performs track to track stepping timing, head load timing, serial to parallel data conversion; parallel to serial data conversion; error code checking/generation, and IBM 3740 softsector compatible recording. After each operation is completed, the chip can optionally interrupt the CPU. (For complete description, see Western Digital FD1795 specification). I/O ports 64,65,66 and 67 are contained within this device.

The FD1795 also has the necessary signals to implement double density operation including a pin to determine whether the chip is to operate single or double density and a late and an early signal for use in precompensation.. The FD1795

has a negative true data bus.

2-3 DATA OUT BUS

The 8 bit DATA OUT BUS is the S-100 path for transferring data from the computer (CPU) to the output ports on the VERSAFLOPPY II board.

2-4 DATA IN BUS

The 8 bit DATA IN BUS is the S-100 path for transferring data from the input ports on the VERSAFLOPPY II board to the computer (CPU).

2-5 A0-A7

The A0-A7 low order eight address lines are used by the computer (CPU) to select the various input/output ports on the board.

2-6 I/O CONTROL LINES AND READ/WRITE CONTROL

The I/O Control lines consist of $\overline{\text{PWR}}$, PDBIN, SOUT, SINP. These lines are used to control the input and output operations from/to the I/O ports on the board.

2-7 WAIT STATE CONTROL AND PRDY

The Wait State Generator is used by the VERSAFLOPPY II to delay the input and output operations until the FD1795 chip is ready to transfer a word. This PRDY line puts the CPU in a wait state during the delay. Wait states are only generated during sector reads and writes (which use I/O port 67).

2-8 ADDRESS DECODER

The Address Decoder detects when a port address used on the VERSA FLOPPY II is present on the low order eight bits of address from the CPU (A0-A7). The output of the decoder is used to gate read and write pulses to the I/O ports.

2-9 DATA IN BUFFER

The Data In Buffer isolates the Bi-Directional Data Bus used on the VERSAFLOPPY II from the S-100 Data In Bus. This buffer is enabled during input port reads from ports on the VERSAFLOPPY II. The data is inverted by the Data In Buffer to compensate for the negative true data bus of the FD1795 controller chip.

2-10 DATA OUT BUFFER

The Data Out Buffer isolates the Bi-Directional Data Bus used on the VERSAFLOPPY II from the S-100 Data Out Bus. This buffer is enabled except during input port reads from ports on the VERSAFLOPPY II. The output data is inverted by the Data Out Buffer to compensate for the negative true data bus of the FD1795 controller chip.

2-11 BI-DIRECTIONAL DATA BUS

The Bi-Directional Data Bus is a path for all transfers to and from the I/O ports on the VERSAFLOPPY II.

2-12 INTERRUPT CONTROL

The VERSAFLOPPY II operates with or without interrupts, but the standard control software does not use interrupts.

2-13 OUTPUT PORT 63

Output Port 63 is an 8 bit control register with several functions:

1. Bits 0-3 Drive Select 1,2,3,4
2. Bit 4 Side Select for double sided drives
3. Bit 5 5"/8" drives
4. Bit 6 Double/Single Density
5. Bit 7 Wait State Enable/INUSE STB*

*The $\overline{\text{INUSE}}$ STB when set low during drive select activation/deactivation will lock or unlock the drive door if that option is incorporated on the drive. This function can be disabled by cutting the etch between E11 and E12.

2-14 INPUT PORT 63

Input Port 63 is used to read the present state of several control signals:

1. Bits 0-7 State of Output Port 63, as described above

2-15 SELECT BUFFER

The Select Buffer supplies the current sinking drive for the drive and side select lines.

2-16 CONTROL BUFFER

The Control Buffer supplies the current sinking drive for $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{DIRECTION}}$, $\overline{\text{STEP}}$, $\overline{\text{TRK43}}$, and $\overline{\text{HLD}}$.

2-17 SENSE BUFFER

The Sense Buffer receives the $\overline{\text{READ DATA}}$, $\overline{\text{INDEX}}$, $\overline{\text{TRK00}}$, $\overline{\text{READY}}$, and $\overline{\text{WRTPRT}}$ signals from the selected disk drive. Each input is a Schmitt Trigger providing hysteresis noise immunity.

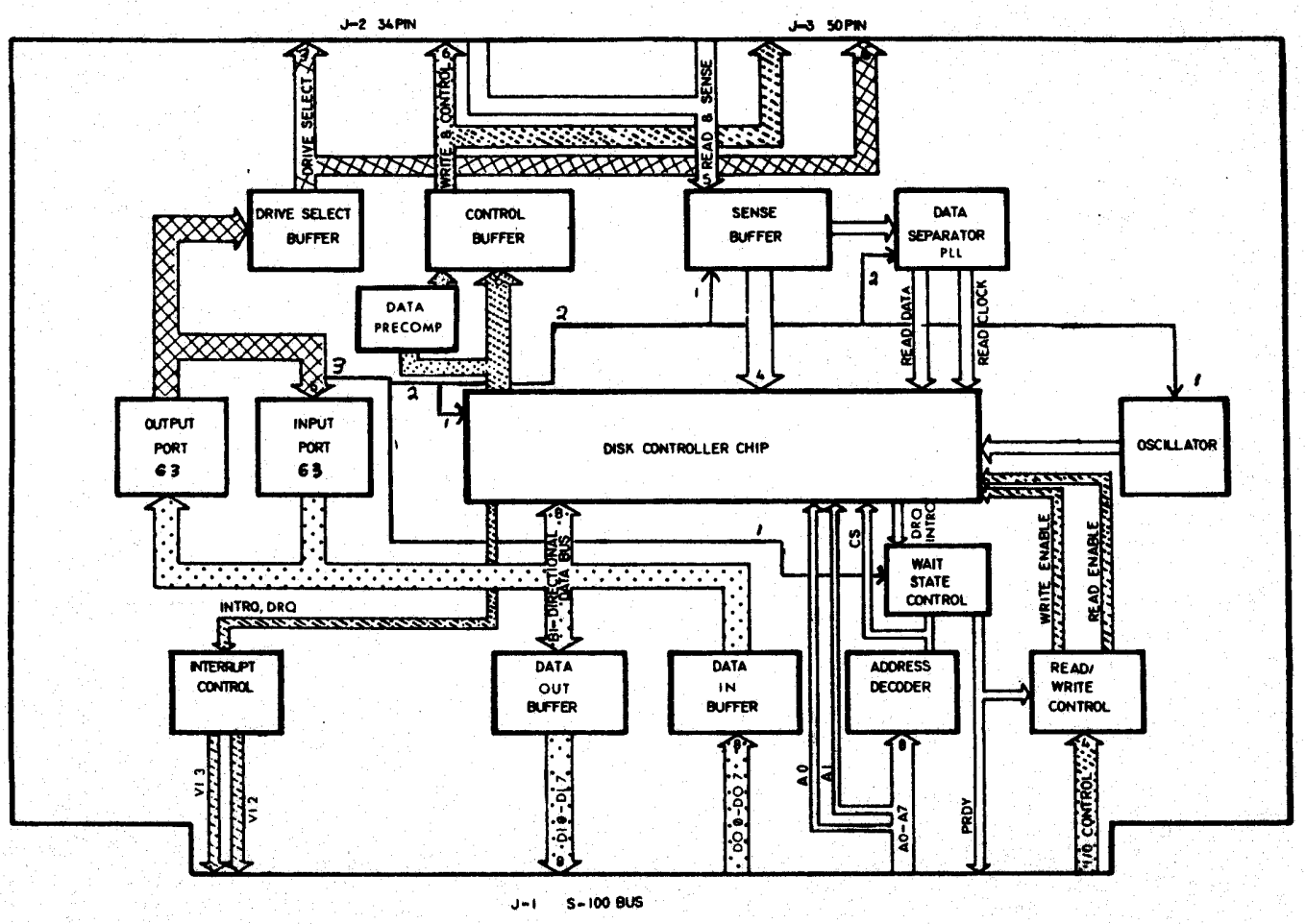
2-18 DATA SEPARATOR

The Data Separator circuit divides the composite FM & MFM READ DATA

into separated Data and Clock signals required by the FD1795 controller chip. The data separator uses the 74LS124 VCO coupled with a LM301 OP AMP to dynamically reconstruct the data clock from the input raw data stream.

2-19 OSCILLATOR

The Oscillator circuit provides a crystal controlled squarewave (16MHZ) divided down to provide the proper clock frequency to the FD1795 for 8" or 5 1/4" operation.



VERSAFLOPPY II BLOCK DIAGRAM

FIGURE 2-1

TABLE 2-1

S-100 BUS SIGNALS USED BY VERSAFLOPPY II

PIN	SIGNAL NAME	DIRECTION	DESCRIPTION
1,51	+8Volts		
2	+16 Volts		
6	VI2	OUTPUT	INTERRUPT CHANNEL 2 (OPTIONAL)
7	VI3	OUTPUT	INTERRUPT CHANNEL 3 (OPTIONAL)
24	Ø2	INPUT	PHASE 2 CLOCK
25	Ø1	INPUT	PHASE 1 CLOCK
29-31, 79-83	A0-A7	INPUTS	OW ORDER ADDRESS
35,36,38-40,88-90	DOØ-DO7	INPUTS	DATA OUT BUS
41-43, 91-95	DIØ-DI7	OUTPUTS	DATA IN BUS
45	SOUT	INPUT	PORT OUTPUT CYCLE
46	SINP	INPUT	PORT INPUT CYCLE
72	PRDY	OUTPUT	READY
77	$\overline{\text{PWR}}$	INPUT	WRITE
78	PDBIN	INPUT	DATA BUS IN
99	$\overline{\text{POC}}$	INPUT	POWER ON CLEAR
100,50	GROUND		

SECTION III

CONTROL SOFTWARE

3-1 INTRODUCTION

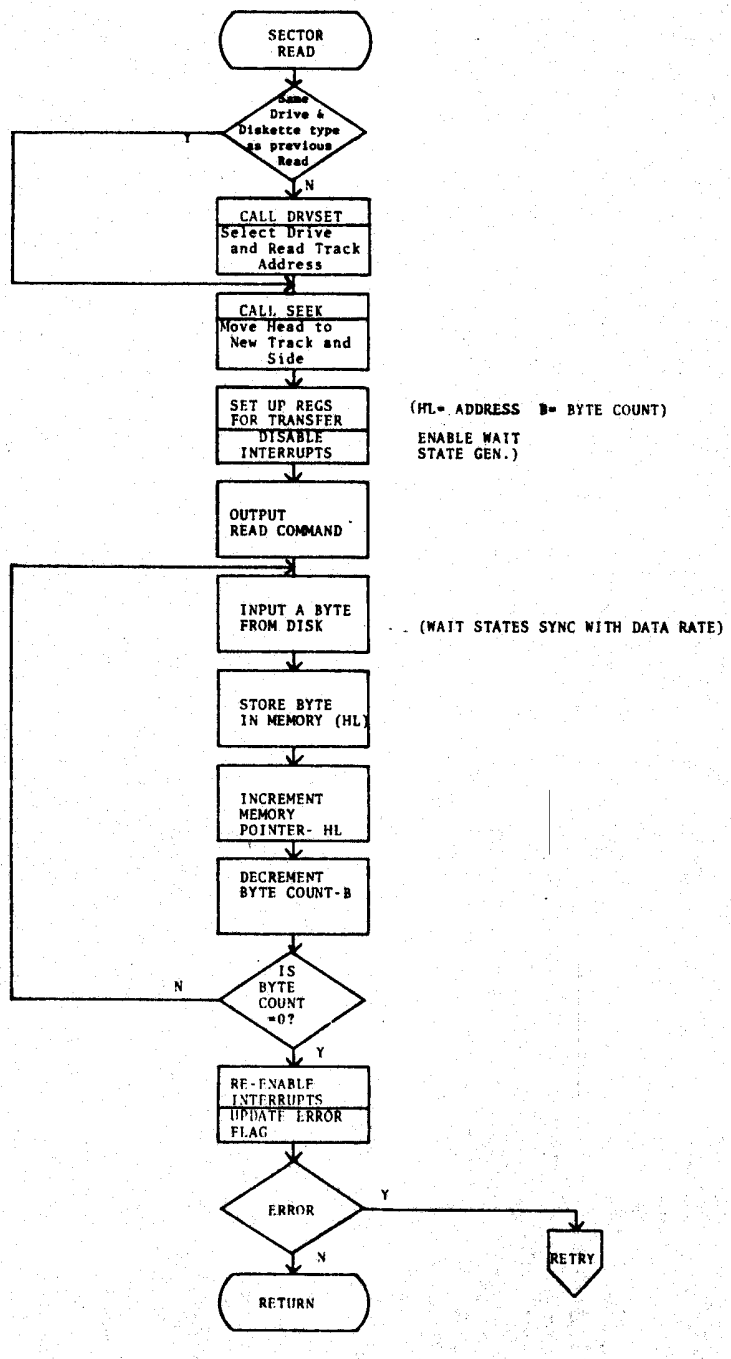
The versatility of the VERSAFLOPPY II is maintained by its ability to be controlled by software. Certain sequences must be executed to ensure proper operation of the disk drive. These control sequences are supported by the SD SYSTEMS' DDBIOS software program. This section will cover these basic software sequences with verbal and graphic description. Program listings of the software in Z-80 source code are included in Appendix E.

The SECTOR READ and SECTOR WRITE sequences are the two main entries into the controlling software. Before these sequences may be entered, the memory transfer address, drive select, track, and sector must have been stored in memory locations. When operating with SDOS Disk Operating System, these parameters are set up when the SETDMA, SELDSK, SETTRK, and SETSEC entries, respectively, are called. The READ and WRITE SDOS entries are linkages to the SECTOR READ and SECTOR WRITE sequences, respectively. If an error is encountered in the Read or Write process, two more attempts will be made to execute the process. After this a Reseek will be executed and then three more Retrys. If an error still exists, program control will be returned to the user with the Z bit reset. If no error exists the Z bit will be set upon Return.

3-2 SECTOR READ SEQUENCE (Figure 3-1)

The function of the SECTOR READ SEQUENCE is to do everything necessary to transfer the previously specified sector (128 BYTES) to the previously specified memory buffer (anywhere in the system RAM):

SECTOR READ SEQUENCE
FIG 3-1



SECTOR READ SEQUENCE

FIGURE 3-1

The UNIT byte is compared to the unit check byte to determine if the desired drive and diskette type is the same as the previously selected drive and diskette type. If not, the DRVSET routine is called to set up the new drive and determine the diskette type table address to be stored in the IX index register. If DRVSET is called then ID READ is also called to set up the track address of the new drive.

The SEEK and TRINT (section 3-5) subroutines are called to put the Read/Write head on the requested side and track.

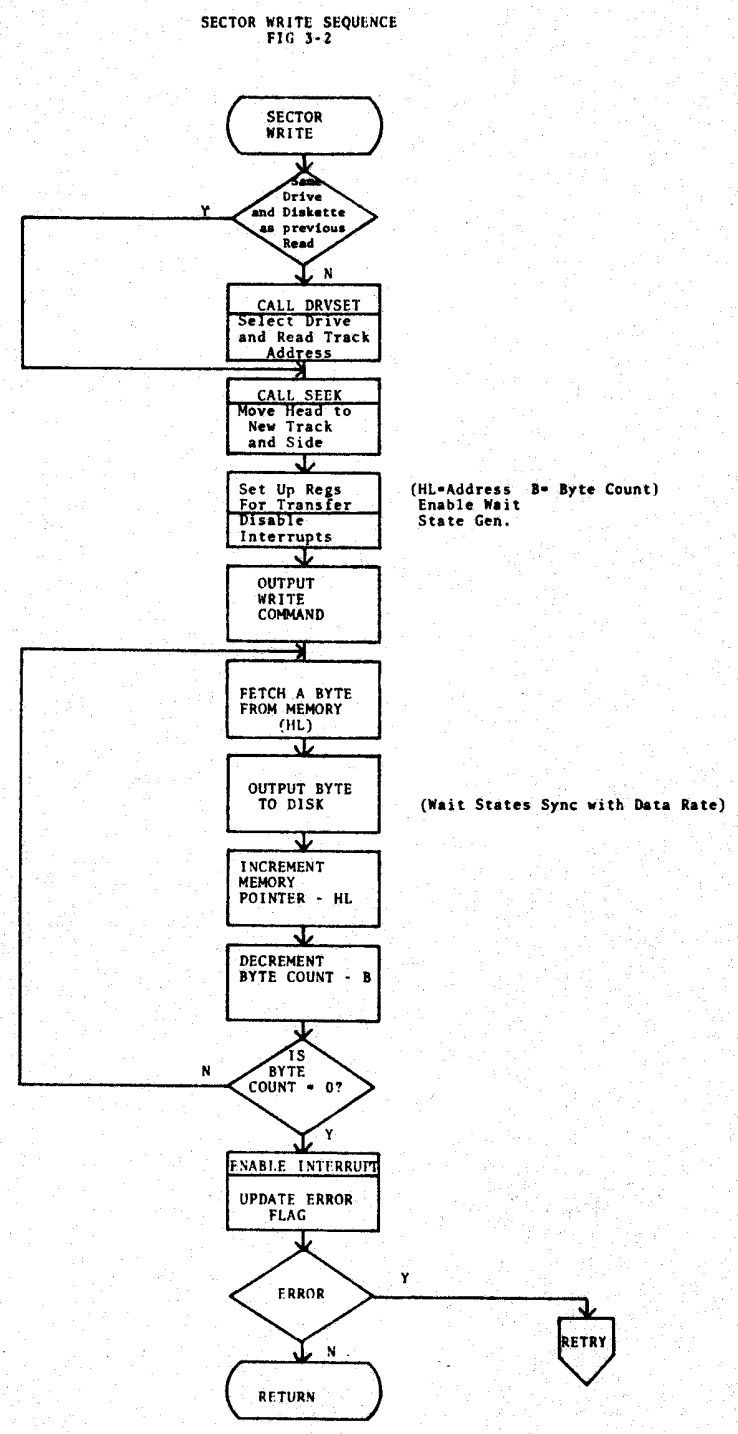
The CPU registers are then set up with the memory address and byte count. Data from the disk is input a byte at a time, and stored in memory. This process is synchronized with the disk data rate by hardware inserted wait states. (Interrupts are dis-abled during data transfers).

When all 128 bytes of data have been read in, the program waits for the hardware to go "not busy". The End of Command Routine then checks for CRC and other error conditions. If no errors occured, the program returns to the caller with the error flag cleared.

3-3 SECTOR WRITE SEQUENCE (figure 3-2)

The function of the SECTOR WRITE SEQUENCE is to do everything necessary to transfer the previously specified memory buffer (128 bytes anywhere in the system) to the previously specified disk sector.

The UNIT byte is compared to the unit check byte to determine if the desired drive and diskette type is the same as the previously



SECTOR WRITE SEQUENCE

Figure 3-2

selected drive and diskette type. If not, the DRVSET routine is called to set up the new drive and determine the diskette type table address to be stored in the IX index register. If DRVSET is called then ID READ is also called to set up the track address of the new drive.

The SEEK and TRINT (section 3-5) subroutines are called to put the Read/Write head on the requested side and track.

The CPU registers are then set up with the memory address and byte count. The data is output a byte at a time, to the disk. This process is synchronized with the disk rate by hardware inserted wait states. (Interrupt are disabled during data transfers).

When all 128 bytes of data have been output, the program waits for the hardware to go "not busy". The End of Command Routine then checks for CRC and other error conditions. If no errors occurred, the program returns to the caller with the error flag cleared.

3-4 DRIVE SELECTION SEQUENCE (Figure 3-3)

The DRIVE SELECTION SEQUENCE translates the data in the unit byte into the format of the select register. The IX index register is then set up with the diskette type table address desired. The new selection is output followed by a delay for Drive Select. This delay is 18 milliseconds for a full-size drive and about 50 milliseconds for a mini.

The status is then read to verify that the drive is ready. If the drive is not ready, the error exit is taken.

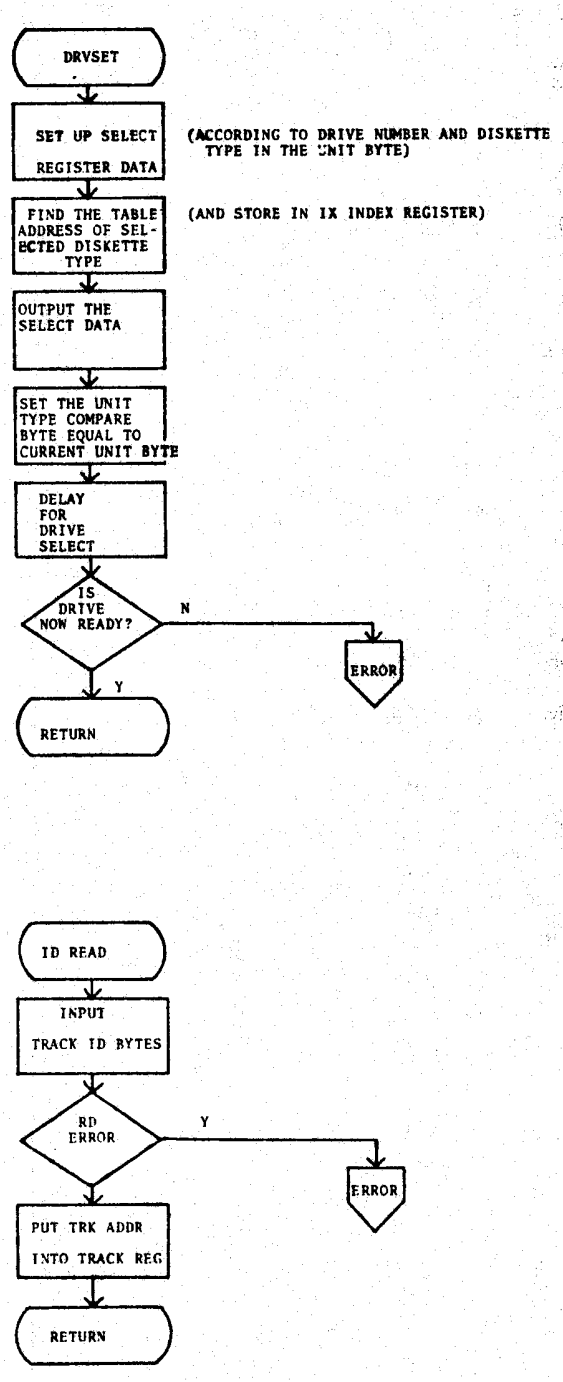
ID READ

In the ID READ ROUTINE the track address is read from the disk to inform the hardware of what track the new drive's read/write head is presently on. The normal return routine is then executed.

3-5 TRACK SEEK AND TRANSFER INITIALIZATION

The TRACK SEEK routine moves the head to the proper track, after verifying the track is valid. The TRANSFER INITIALIZATION (TRINT) sequence is responsible for verifying that the requested sector is a valid number and in the case of the double-sided drives, select the proper side of the disk. The Transfer Address is also set up in this routine.

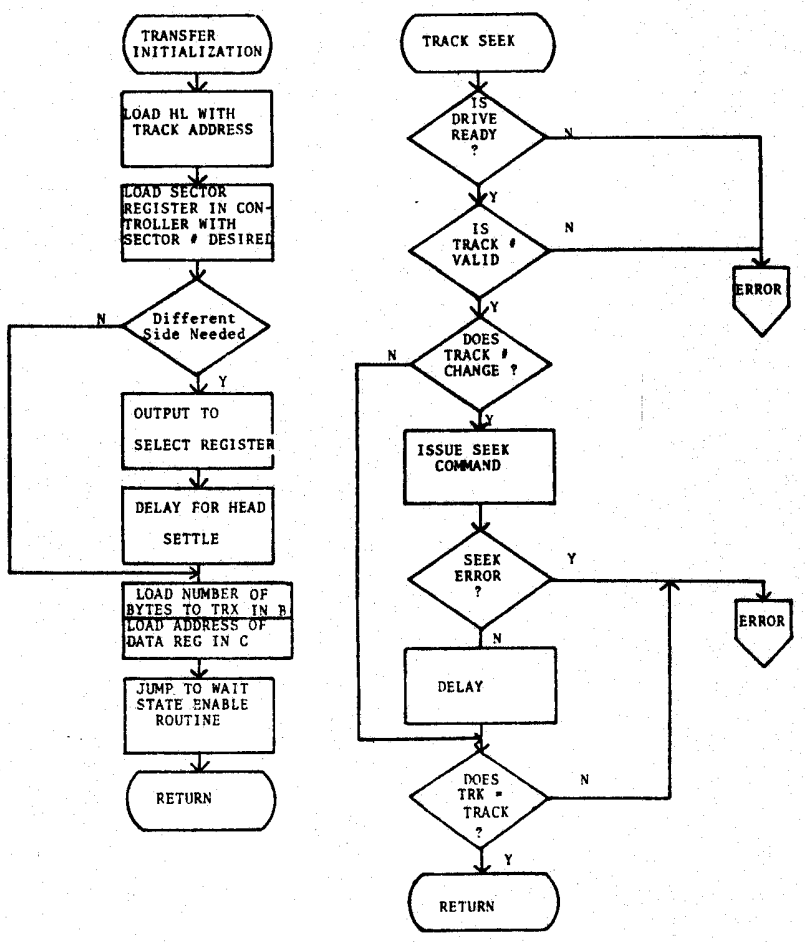
DRIVE SELECTION SEQUENCE
FIG 3-3



DRIVE SELECTION SEQUENCE

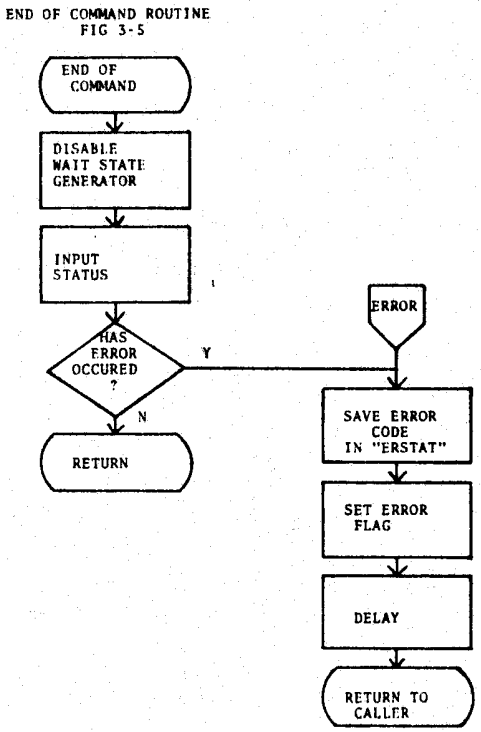
Figure 3-3

TRACK SEEK AND TRANSFER INITIALIZATION
FIG 3-4



TRACK SEEK

Figure 3-4



END OF COMMAND ROUTINE

Figure 3-5

3-6 END OF COMMAND ROUTINE (figure 3-5)

The END OF COMMAND ROUTINE is entered after both normal and error terminations of hardware executed commands. The routine waits for the FD1795 to become "not busy". The wait state generator is then disabled, and the status is input to check for errors. If no error occurred, then a normal return is taken.

If an error condition is detected, then error type is saved, error flag set and a return is taken directly back to the caller after a delay (18 MS-8"; 50 MS-5")

3-7 FORMAT ROUTINE

The FORMAT ROUTINE is entered directly through the vector at location FØ33. This routine expects the UNIT byte to be set up previously according to the type of format desired. See Table 8-1 for valid UNIT byte data.

NOTE 1: The DDBIOS software uses the side byte on the diskette to determine if the diskette is single or double sided. It therefore may mis-read disks formatted double-sided on an SD-100 as single-sided.

NOTE 2: Early boards used a 1791B-1 controller chip, which is not able to read disks formatted with all zeros in the gaps between sectors. Therefore, VersaFloppy II boards with the 1791B-1 cannot read disks formatted by machines with a 1771 controller chip (like the S.D. Systems SD-100).

SECTION IV

CONSTRUCTION

4-1 INTRODUCTION

The SD SYSTEMS VERSAFLOPPY II kit is intended for those people who have had some prior experience with kit building and digital electronics. If you do not fall into this category it is highly recommended that you find an experienced person to help you in assembly and check out of the board.

Appendix B shows the parts list for the SD SYSTEMS Floppy Disk Controller board. Double check all parts against this parts list.

4-2 ASSEMBLY PROCEDURE

1. Install and solder the IC sockets in their proper locations as follows: (Do not install sockets in U1 or U2)

   14 Pin at U4,8,11,12,14-18,21-26,32-34
   16 Pin at U5-7,13,19,20
   20 Pin at U9,27-31
   40 Pin at U10

2. Install and solder the resistors as follows: All are ¼W, 1% (except as noted) and the values are given in Ohms.

A.	R15	120	(Brown,Red,Brown) 5%
B.	R3,R6,R7,R8,R9	150	(Brown,Green,Brown) 5%
C.	R31	200	
D.	R32	301	
E.	R33	680	(Blue,Gray,Brown) 5%
F.	R4,R22	1K	(Brown,Black,Red)
H.	R19	1.1K	(pot)
I.	R16,R24	2.2K	(Red,Red,Red) 5%
J.	R29,R30	4.22K	
K.	R2,R23	5.11K	
L.	R13	5.6K	(Green,Blue,Red) 5%
M.	R25	7.32K	
N.	R5,R11,R12	10K	(Brown,Black,Orange) 5%
O.	R1,R27	15K	
P.	R10	47K	(Yellow,Violet,Orange) 5%
Q.	R18,R26	100K	
R.	R17,R21	9.094K	

3. Install and solder diodes with the banded end as shown on the PC board.

   A. Install and solder CR1 Zener Diode 1N4742A-12V
   B. Install and solder CR2,CR3 Diode 1N270
   C. Install and solder CR4-CR6 Diodes 1N914
   D. Install and solder CR7 5V Zener Diode 1N751A

4. Install and solder the capacitors as follows:

A.	C1,C27	.047 MF
B.	C2,C28	.015 MF
C.	C3	150 pf
D.	C4-C13,C16,C20-C26,C32,C35-37	.1 uf
E.	C14,C17-C19,C34	10 MF
F.	C15	47uf
G.	C29	100 pf
H.	C30	.001 MF
I.	C31	4.7 MF
J.	C33	47 pf

5. Install and solder the voltage regulator with the heatsink using the 6-32 hardware supplied.

   VR1 +5V 7805 or LM340T-5

6. Install the W/W pins in TP 1-TP 3 and TP 5.

7. Install and solder 100 UH RF choke.

8. Install and solder J2 (34 pin) and J3 (50 pin) connectors.

9. Double check all solder connections for cold solder joints, unsoldered connections or shorted connections.

4-3 VOLTAGE CHECK

1. Install the board in the computer and measure the output of +5V regulator VR1 and +12V of CR1.

   VR1 = +5V (Pin 3)
   CR1 = +12V (Cathode)

2. Measure the power supply voltages in the Floppy Disk Controller chip.

   A. Pin 21 U16 = +5V
   B. Pin 40 U16 = +12V

NOTE: Do not proceed with the board check out until all power supply voltages are correct. The TTL and MOS logic can be permanently damaged if improper voltages are applied.

3. Install the IC's in their sockets observing the PIN 1 designation on each socket marked on the PC board. NOTE: U10's ORIENTATION IS DIFFERENT FROM THE OTHER IC's. Also, on U1 the manufacturer's symbol designates Pin 1. On U2 the dot below the triangle designates the corner of the chip that contains pin 1.

A.	U21	74LS00
B.	U23,U33	74LS02
C.	U8,U32	7406
D.	U14	74LS09
E.	U24,U26	74LS10
F.	U11,U15,U17	74LS14
G.	U16	74LS21
H.	U12	74LS32
I.	U22,U25,U34	74LS74
J.	U4,U18	74LS93
K.	U6	74LS112
L.	U13	74LS124
M.	U5	74LS153
N.	U20	74LS157
O.	U7,U19	74LS221
P.	U28,U29	74LS240
Q.	U9,U27,U30	74LS244
R.	U31	74LS273
S.	U10	FD1795B
T.	U3	LM 301 AN

4. Install and solder delay line (DDU-4-2400) in location U2.

5. Install and solder 16MHZ oscillator in location U1.

6. Install PCB ejectors using mounting pins (see Assembly Drawing).

4-4 PHASE LOCKED OSCILLATOR ADJUSTMENT

1. Connect an oscilloscope probe to TP 3.

2. Set the timebase to display 500NS/DIV.

3. Adjust the variable resistor R-19 until there are 10 pulses displayed on the oscilloscope screen.

4. Adjust the variable resistor R-19 until the leading edge of the first pulse is exactly lined up on the first division line on the oscilloscope screen and the trailing edge of the last pulse is exactly lined upon the last division line on the oscilloscope screen.

SECTION V

INTERRUPT OPTIONS

5-1 INTRODUCTION

There are basically two possible methods of handling interrupts with the VERSAFLOPPY II:

1. Interrupts are not used. (Standard Software)
2. Z-80 Mode 2 using CTC interrupt circuit on SBC-100/200

The Standard Control Software does not use interrupts. However in some cases it may be beneficial to issue a command (such as SEEK TRACK) and be interrupted when it is complete.

SECTION VI

SOFTWARE OPTIONS

6-1 INTRODUCTION

The standard control software for the VERSAFLOPPY II is supplied in listing form (Appendix D) and also available in 2716 PROM for an additional charge. This software is called DDBIOS (Double Density Basic I/O System) and is assembled to reside at F000H.

6-2 BOOTING UP THE SDOS

In order to run SDOS, a minimum of 16K of RAM must be in the system starting at address 0000 and the BIOS PROM must be at F000H. Execute BIOS at F000 and SDOS will be booted and promp with "[A]". Refer to the "SD SYSTEMS DISK OPERATING SYSTEM (SDOS) USER'S GUIDE" for details of the SDOS commands.

SECTION VII

CHECK - OUT

7-1 INTRODUCTION

This section will describe some basic checks that should be made on the VERSAFLOPPY II. NOTE: It is assumed at this point that the voltage checks described in Section 4 have been previously made. The following checks require that the CPU board also be plugged into the Bus.

7-2 OSCILLATOR

Apply power to board and verify that there is a 16MHZ clock on U9 - Pin 3.

7-3 $\overline{RE}$ AND $\overline{WE}$ PULSES

Verify that U10 Pin 4 pulses low during any Input instruction, and U10 Pin 2 pulses low during any output instruction.

7-4 I/O PORT WRITE/READ VERIFICATION

Using the monitor in the system or a short program, write data to port 65 and read it back. Verify that the data read back is the same as that written. This is done to test the data path to and from the FD1791B-1 as well as the internal register. REPEAT this procedure for ports 66, 67 and 63.

7-5 HEAD LOAD MONOSTABLE

After the diagnostic software is operating, check U20-Pin 3 for a 35 millisecond pulse (low) and U20-Pin 2 for 1.5 sec pulse (low) each time the head loads.

SECTION VIII

DIAGNOSTIC SOFTWARE

8-1 INTRODUCTION

A diagnostic program for the VERSAFLOPPY II is supplied in the top of the 2716 DDBIOS PROM. The diagnostic program is also on the diskette, when SDOS is purchased, under the file name of "VFDIAG.COM" Once SDOS is operating, the diagnostic may be run by typing VFDIAG (CR). THE SDOS DISKETTE SHOULD NOT BE PLACED IN THE DRIVE UNTIL THE VERSAFLOPPY II AND DISK DRIVES HAVE BEEN THOROUGHLY CHECKED OUT.

When running the diagnostic to check-out the VERSAFLOPPY II, execute the program starting at address F600. The diagnostic uses the DDBIOS and monitor PROMS for disk and console I/O.

8-2 DIAGNOSTIC TEST START-UP

Upon executing the diagnostic program the following message will print on the console:

TEST# DRV# (TTDD)

The program then waits for the test number and drive number to be entered from the console followed by a carriage return.

NOTE: The test number and drive number are each two digits and MUST NOT be separated by a comma or space. Table 8-1 shows drive numbers.

Type / Drive	#Sides Disk Size Density	1 Full Single	2 Full Single	1 Mini Single	2 Mini Single	1 Full Double	2 Full Double	1 Mini Double	2 Mini Double
A		00	10	20	30	40	50	60	70
B		01	11	21	31	41	51	61	71
C		02	12	22	32	42	52	62	72
D		03	13	23	33	43	53	63	73

TABLE 8-1

Note that these unit numbers must also be used with R, W and Z commands in the SD Monitor.

The test routines (except for 05) may be terminated at any time by entering a period (.) on the console keyboard. The diagnostic will then print the above prompting message and wait for further keyboard entries. If the period (.) is entered instead of a command, control will be transferred to the monitor.

8-3 DIAGNOSTIC TEST 00 (SEEK TEST)

Test 00 is a simple routine to verify that the VERSAFLOPPY II is receiving commands properly and that the track seek circuitry is functional. The selected drive should begin moving the head from track 00 to the inside track (76 for full size, 34 for mini) and back again. Enter a period on the keyboard to cause the test to cease.

8-4 DIAGNOSTIC TEST 01 (WRITE/READ)

Diagnostic test 01 writes random data on each sector, reads the

sector back and compares the data to verify that it is identical. Any errors which occur will be printed on the console. (see Section 8) This is done to each sector sequentially, starting at track 00, sector 1, until reaching the innermost track. At that point it prints a "P" on the console, returns to track 00, and continues.

NOTE: Diagnostic tests which read and write to disk may only be run after the diskette has been formatted using diagnostic 05. (see 8-8)

8-5 DIAGNOSTIC TEST 02 (READ TEST)

Test 02 reads every sector on the disk sequentially and checks for CRC errors, and seek errors. Errors will be reported on the console. This test should step from track to track at the same rate as when formatting a diskette.

8-6 DIAGNOSTIC TEST 03 (RANDOM WRITE/READ)

This test is similar to test 01 in that it writes, reads and compares data byte by byte. However, test 03 chooses the sectors and tracks on a random basis in an attempt to simulate actual use. This test exercises only on the specified drive.

8-7 DIAGNOSTIC TEST 04 (MULTI-DRIVE RANDOM WRITE/READ

This test is identical to test 03 except that it also selects a random drive (0 or 1).

8-8 DIAGNOSTIC TEST 05 (FORMATTING)

Test 05 is actually not a diagnostic, but a program which formats a diskette in accordance with drive and density type. This must be done to all diskettes before further use. Note that on the distributed SDOS diskette there is a program which formats a diskette. This program has the filename "FORMAT.COM" and may be run by entering "FORMAT (CR)". BE SURE TO USE A SCRATCH OR UNFORMATTED DISKETTE WHEN FORMATTING BECAUSE ANY PREVIOUSLY WRITTEN DATA WILL BE LOST.

8-9 DIAGNOSTIC TEST FF (JUMP)

Test code FF allows exiting the diagnostic to anywhere in memory. The following sequence describes this:

CONSOLE INTERACTION	COMMENTS
TEST # DRV # (TTDD): FF00 (CR) ADDRESS: 3000 (CR)	Jump to address 3000H

8-10 DIAGNOSTIC ERROR REPORTING

If any errors occur during diagnostics 1,2,3, or 4, the errors will be reported on the console as follows:

CMD STAT DRV TRK SCTR CC SS DD TT SS

where CC = The controller command being executed
SS = The error status (type of error)
DD = The drive being tested
TT = The track being tested
SS = The sector being tested

Table 8-1 lists all the various controller commands and Table 8-2 contains the definition of each bit in the error status byte.

TABLE 8-1

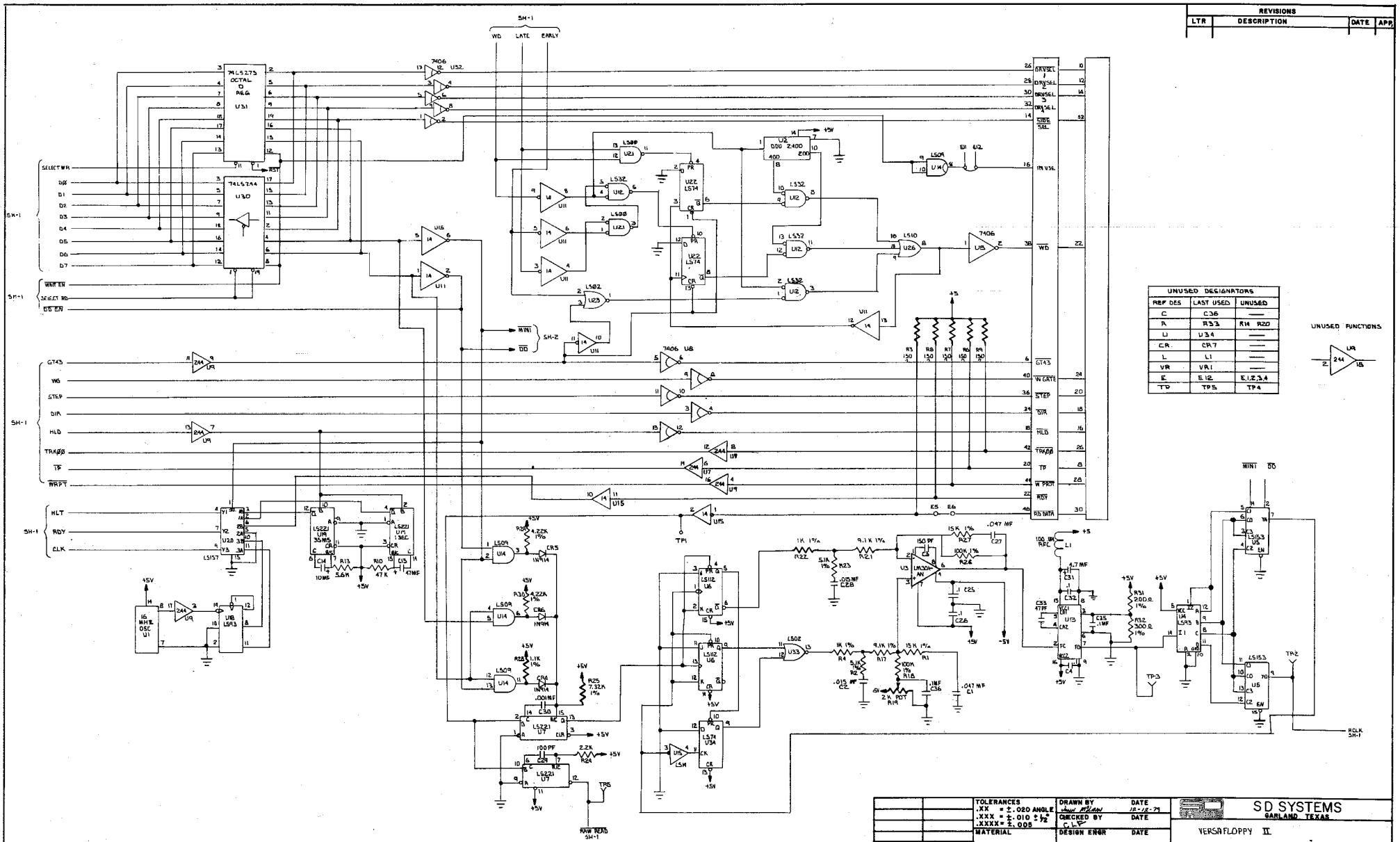
DISK CONTROLLER COMMAND CODES

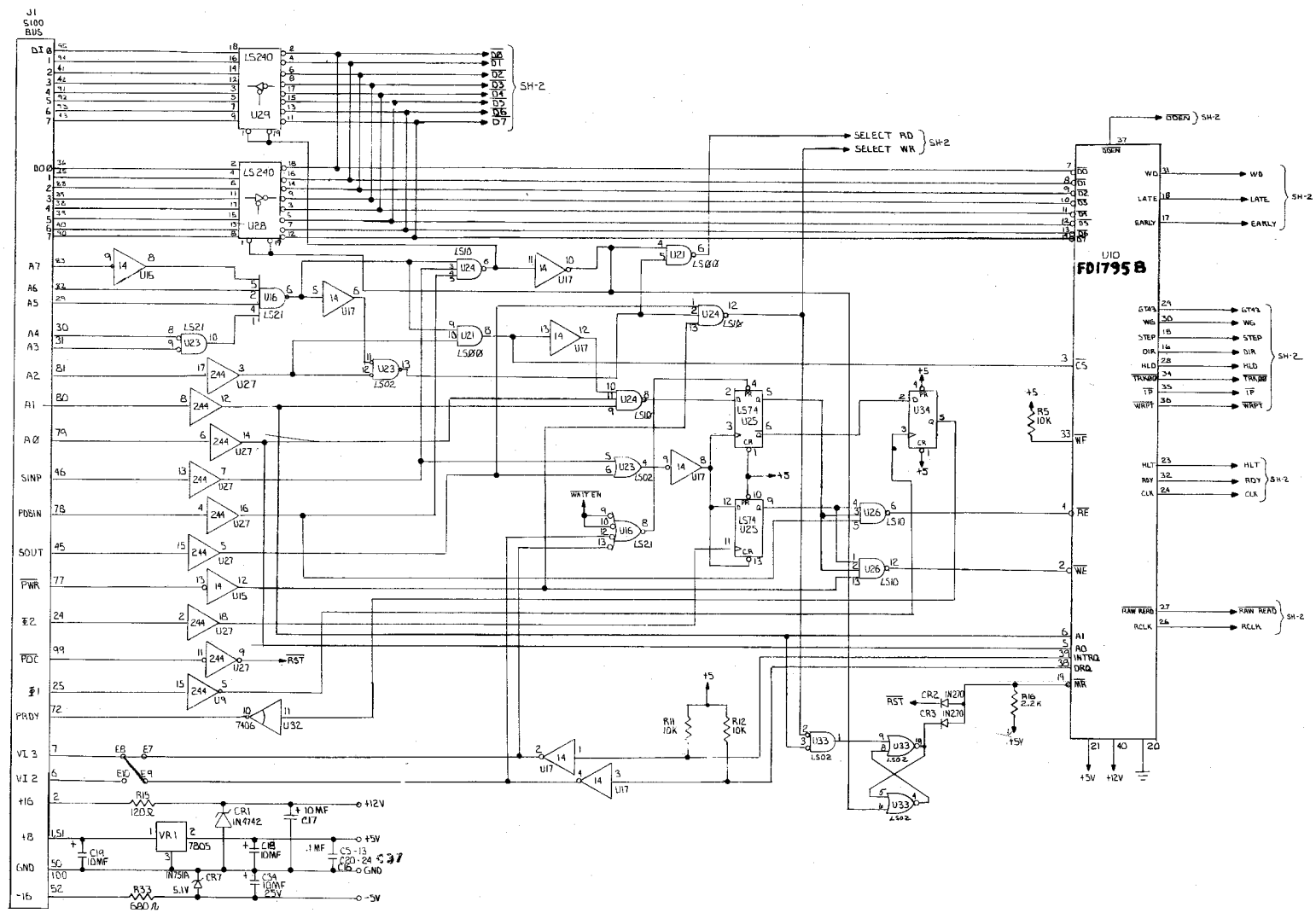
MINI DISK CMD CODE	FULL SIZE CMD CODE	DESCRIPTION
0B	09	Restore Drive TRK ØØ
13	19	Track Seek with No Verify
F4	F4	Format Track
88	80	Read Sector
A8	AØ	Write Sector
C4	CØ	Read Track Address

TABLE 8-2

ERROR STATUS DEFINITION

BIT #	DEFINITION
BIT Ø	Busy
BIT 1	DRQ Bit (Indicates Excessive noise on S-100 Bus)
BIT 2	Data Lost
BIT 3	CRC Error
BIT 4	Sector Not Found
BIT 5	Track Seek Error
BIT 6	Write Protected Diskette
BIT 7	Drive Not Ready
FE	Controller Hang Up
ØF	Invalid, Track Error


REVISIONS
LTR | DESCRIPTION | DATE | APP
UNUSED DESIGNATORS
REF DES | LAST USED | UNUSED
C | C36 | —
R | R33 | R14 R20
U | U34 | —
CR | CR7 | —
L | L1 | —
VR | VR1 | —
E | E12 | E1,2,3,4
TP | TP5 | TP4
UNUSED FUNCTIONS
74LS273 OCTAL D REG U31
74LS244 U30
SELECT WR
WRITE EN
SELECT RD
DS EN
WD
LATE
EARLY
STEP
DIR
HLD
TRK00
TF
WRPT
HLT
RDY
CLK
RCLK SH-1
TRK READ SH-1
MINI
DD
SD SYSTEMS
GARLAND TEXAS
VERSAFLOPPY II
SCHEMATIC
SIZE D
DRAWING NO. 0100151
REV K
SHEET 2 OF 2
DO NOT SCALE DRAWING
TOLERANCES .XX = ± .020 ANGLE .XXX = ± .010 ± ½° .XXXX = ± .005
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DRAWN BY Jim Nolan DATE 12-12-79
CHECKED BY CLP DATE
DESIGN ENGR DATE
PROJ ENGR DATE
APPROVED DATE
NOTES:



REVISIONS			
LTR	DESCRIPTION	DATE	APP

NOTES:
1. ALL 14'S AND 244's ARE LS
2 ALL LS PARTS ARE 74 SERIES
3 ALL RESISTORS ARE 1/4 WATT 5% EXCEPT AS NOTED

		TOLERANCES .XX = ±.020 ANGLE .XXX = ±.010 ± ½° .XXXX = ±.005	DRAWN BY MKC DATE 12-4-79	SD SYSTEMS GARLAND TEXAS
		MATERIAL	CHECKED BY CLP DATE	VERSAFLOPPY II
			DESIGN ENGR DATE	SCHEMATIC
			PROG ENGR DATE	
		FINISH	APPROVED DATE	SIZE D · CODE IDENT · DRAWING NO. 0100151 · REV K
NEXT ASSY	USED ON			SCALE — · DO NOT SCALE DRAWING · SHEET 1 OF 2
APPLICATION				

SD Systems

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BILL OF MATERIALS

Title: VERSAFLOPPY II	PL No. 0100150	Rev. N
Date Released:	Approved:	Sheet 1 Of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
1	1	7000013	VERSAFLOPPY II PCB # 0100152		
2	18	7060002	14 PIN IC SOCKET U4,8,11,12,14, THRU 18,21 22,24 THRU 26,32 & 33,23 & 34		
3	6	7060003	16 PIN IC SOCKET U5,6,7,13,19 & 20		
4	6	7060005	20 PIN IC SOCKET U9,27 THRU 31		
5	1	7060009	40 PIN IC SOCKET U10		
6	2	7010007	7406 TTL IC U8 & U32		
7	1	7010160	74LS00 TTL IC U21		
8	2	7010162	74LS02 TTL IC U23 & U33		
9	2	7010168	74LS10 TTL IC U24 & U26		
10	3	7010172	74LS14 TTL IC U11, U15 & U17		
11	1	7010175	74LS21 TTL IC U16		
12	1	7010181	74LS32 TTL IC U12		
13	3	7010195	74LS74 TTL IC U22, U25 & U34		
14	2	7010205	74LS93 TTL IC U18 & U4		
15	1	7010225	74LS153 TTL IC U5		
16	1	7010228	74LS157 TTL IC U20		
17	3	7040001	IN914 DIODE CR4, CR5 & CR6		
18	2	7010259	74LS221 TTL IC U7 & U19		
19	2	7010260	74LS240 TTL IC U28 & U29		
20	3	7010264	74LS244 TTL IC U9, U27 & U30		
21	1	7010276	74LS273 TTL IC U31		
22	1	7080006	16 MHZ CRYSTAL U1		
23	1	7010371	DOU 4-2400 DELAY LINE U2		
24	1	7060001	8 PIN IC SOCKET		

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BILL OF MATERIALS

Title: VERSAFLOPPY II	PL No. 0100150	Rev. N
Date Released:	Approved: JS	Sheet 2 Of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
25	1	7020051	120 OHM RESISTOR 5% 1/4 WATT R15		
26	5	7020053	150 OHM RESISTOR 5% 1/4 WATT R3, R6, R7, R8 & R9		
27	2	7130072	PCB EJECTOR		
28					
29	1	7020091	5.6 K OHM RESISTOR 5% 1/4 WATT R13		
30	3	7020097	10K OHM RESISTOR 5% 1/4 WATT R5, R11 & R12		
31	1	7020113	47K OHM RESISTOR 5% 1/4 WATT R10		
32	22	7030045	1 MF CAPACITOR C4 TO C13, C16, C20 TO C26, C32 & C35 TO C37		
33	5	7030009	10 MF 25V CAPACITOR C14, C17, C18, C19 & C34		
34	1	7030010	47 MF CAPACITOR C15		
35					
36					
37	1	7040004	IN4742 12V ZENER DIODE CR1		
38	1	7160001	LM340T-5 VOLTAGE REGULATOR VR1		
39	1	7130005	HEATSINK		
40	1	7130015	6-32 x 5/16 PPH SCREW		
41	1	7130007	6-32 HEX NUT		
42	4	7170001	WIRE WRAP PINS TP1, 2, 3 & 5		
43	1	7090043	CONNECTOR 34 PIN J2		
44	1	7090042	CONNECTOR 50 PIN J3		
45	4	7130078	FLOPPY CABLE EJECTOR CLIPS		
46	1	7010391	FD-1795B FLOPPY CONTROLLER U10		
47	2	7040011	DIODE CR2 & CR3, IN270		
48	2	7020081	2.2K OHM RESISTOR 5% 1/4 WATT R16 & R24		

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BILL OF MATERIALS

Title: VERSAFLOPPY II	PL No. 0100150	Rev. N
Date Released:	Approved:	Sheet 3 Of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
49	1	7010401	74S09 TTL IC U14		
50	1	7010210	74LS112 TTL IC U6		
51	1	7020200	2KΩ POT R19		
52	1	7010404	74LS629 TTL IC U13 (OR 74LS124)		
53	1	7160009	LM 301AN OPERATION U3		
54	2	7020193	4.22K 1% ¼WATT RESISTOR R29 & R30		
55	1	7020192	1.1K 1% ¼WATT RESISTOR R28		
56	1	7020195	7.32K 1% ¼ WATT RESISTOR R25		
57	2	7020191	1K 1% ¼ WATT RESISTOR R4 & R22		
58	2	7020194	5.11K 1% ¼ WATT RESISTOR R2 & R23		
59	2	7020196	9.094K 1% ¼ WATT RESISTOR R17 & R21		
60	2	7020197	15K 1% ¼ WATT RESISTOR R1 & R27		
61	2	7020198	100K 1% ¼ WATT RESISTOR R18 & R26		
62	1	7020189	200Ω 1% ¼ WATT RESISTOR R31		
63	1	7020190	301Ω 1% ¼ WATT RESISTOR R32		
64					
65	1	7020069	680Ω 5% ¼ WATT RESISTOR R33		
66	1	7120002	100 UH RF CHOKE WEE-WEE-100 L1		
67	1	7040003	IN751A 5.1 ZENER DIODE CR7		
68	1	7030035	.001 MF CAPACITOR C30		
69	1	7030004	100 PF CAPACITOR C29		
70	2	7030037	.015 MF CAPACITOR C2 & C28		
71	2	7030038	.047 MF CAPACITOR C1 & C27		
72	1	7030004	100 PF CAPACITOR C33		

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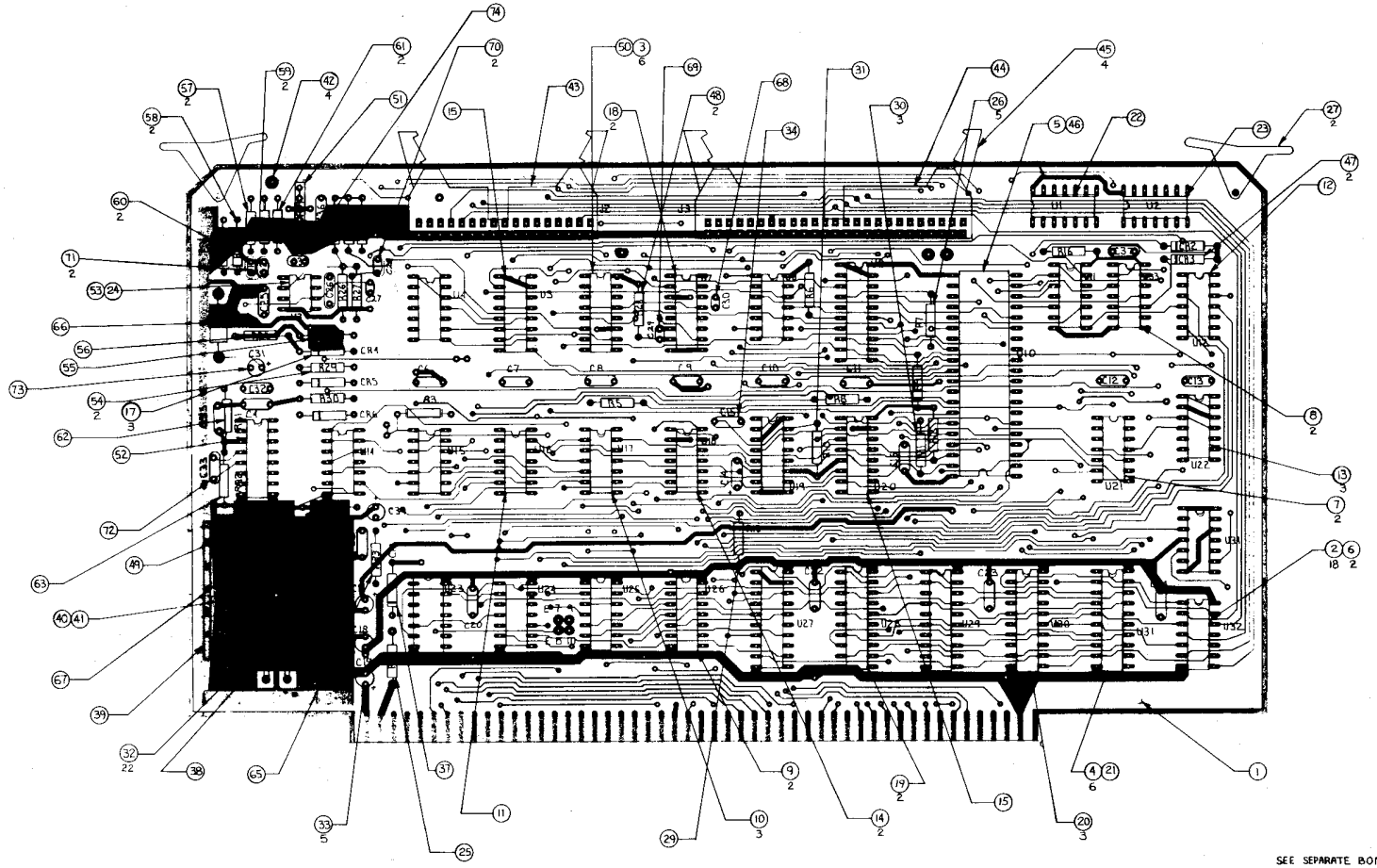
BILL OF MATERIALS

Title: VERSAFLOPPY II	PL No. 0100150	Rev. N
Date Released:	Approved:	Sheet 4 of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
73	1	7030041	4.7 MF 25V CAPACITOR C31		
74	1	7030042	150 PF CAPACITOR C3		

REVISIONS			
LTR	DESCRIPTION	DATE	APP.
K	PER ECN # 120, 147		
L	PER ECN # 127		
M	PER ECN # 158 & 156		



SEE SEPARATE BOM 0100150

NOTES:

		TOLERANCES .XX = ± .020 ANGLE .XXX = ± .010 ± ½° .XXXX = ± .005	DRAWN BY [illegible] DATE 2/13/79	SD SYSTEMS GARLAND TEXAS	
		MATERIAL	CHECKED BY CLF DATE 1/4/80	VERSAFLOPPY II ASSY DRAWING	
			DESIGN ENGR DATE		
			PROJ. ENGR DATE		
		FINISH	APPROVED DATE	SIZE D / CODE IDENT / DRAWING NO. 0100150 / REV N	
NEXT ASSY	USED ON			SCALE ~ / DO NOT SCALE DRAWING / SHEET 1 OF 5	
APPLICATION					

VERSAFLOPPY II
SD SYSTEMS
ASSY 010015D REV F