

2.7.2 MODEL 861 MULTIPROCESSOR UNIT

GENERAL DESCRIPTION

The Model 861 MPU is a single board computer with a processor, memory, and two serial I/O ports. It is used to add multi-user capability to the system.

The Model 861 MPU consists of a single printed circuit board that occupies one slot in the Series 5000 or 8000 Computer Systems. Each serial RS-232C port is brought out to a 3M 26-pin header on the I/O panel.

SPECIFICATIONS

Processor:	4MHz Z-80A CPU
Instruction set:	158 instructions
PROM Capacity:	2K bytes
PROM Type:	2716 or equivalent
RAM Capacity:	64K bytes with Parity
RAM Type:	4164 Dynamic
Serial Channels:	Two asynchronous or synchronous channels with modem control
Serial Channel Type:	Z-80A SIO/0 (or Z-80A DART asynchronous only)
Parallel Channel:	24 bit programmable parallel I/O lines compatible with the S-100 bus for host interface
Parallel Channel Type:	8255A PPI
Interval Timers:	4 timers; two for baud rate control and two cascaded for programmable time interval
Timer Type:	Z-80A CTC
Vectored Interrupts:	Internally prioritized vector interrupt structure of the Z-80A microprocessor
Power Requirements:	+ 8 volts @ 800ma +16 volts @ 80ma -16 volts @ 70ma
Operating Environment:	0-55 deg C

CONFIGURING THE 861 BOARD

I/O Address Selection (Location JE)

The most significant bits of the I/O addresses used by the 861 board are assigned values according to the shunts at location JE. If a shunt is on, the corresponding address bit has a '0' value; if a shunt is off, the bit has a '1' value.

JE					
A7	1	o	o	12	
A6	2	o	o	11	
A5	3	o	o	10	
A4	4	o	o	9	
A3	5	o	o	8	
A2	6	o	o	7	

Each 861 board is assigned a unique address according to the table below:

Board	I/O Address		Board	I/O Address	
	Hex	Binary		Hex	Binary
1st	40H	010000XX	9th	E0H	111000XX
2nd	44H	010001XX	10th	E4H	111001XX
3rd	48H	010010XX	11th	E8H	111010XX
4th	4CH	010011XX	12th	ECH	111011XX
5th	50H	010100XX	13th	F0H	111100XX
6th	54H	010101XX	14th	F4H	111101XX
7th	58H	010110XX	15th	F8H	111110XX
8th	5CH	010111XX	16th	FCH	111111XX

Interrupt Level Selection (Location JF)

The interrupt level for the 861 board can be selected by a shunt on JF.

JF					
VI0	1	o	o	16	
VI1	2	o	o	15	
VI2	3	o	o	14	
VI3	4	o	o	13	
VI4	5	o	o	12	
VI5	6	o	o	11	
VI6	7	o	o	10	
VI7	8	o	o	9	

Port A Receive and Transmit Baud Clock Selection (JA)

The shunts at location JA indicate the source of the Receive and Transmit clocks for the serial ports. Normally, pins 1 and 16 are shunted, pins 3 and 14 are shunted, and pins 6 and 11 are shunted together.

JA

- 1o 16 RxDA from RS-232 (Signal BB - Receive Data)
- 2o 15 RxDA from RS-422 (Signal RD - Receive Data)
- 3o 14 RxCA- from Z-80A CTC T0
- 4o 13 RxCA- from RS-232 (Signal DD - Receive Clock)
- 5o 12 RxCA- from RS-422 (Signal RT - Receive Timing)
- 6o 11 TxCA- from Z-80A CTC T0
- 7o 10 TxCA- from RS-232 (Signal DB - Transmit Clock)
- 8o 9 TxCA- from Z-80A CTC T0/2

Port B Receive Clock Selections (JB)

The shunt at JB indicates the source of the 'receive' clock for port B. Normally, pins 1 and 4 are shunted.

JB

- 1o 4 RxDB from RS-232 (Signal BB - Receive Data)
- 2o 3 RxDB from RS-422 (Signal RD - Receive Data)

Reset Disable (Location JD)

A shunt at location JD disables the RESET signal to the 861 board. JD is only shunted during testing; normally there is no shunt.

JD

- 1o Normal mode - shunt off.
- 2o Local 861 test mode - shunt on.

PORT CONNECTIONS

The 861 is connected to the I/O panel using a flat ribbon cable. The pins and signals are given below:

Signal Name	RS-232C Circuit	Pin	
Signal Ground	AB	7	
Transmit Data	BA	2	(Data to MCDEM)
Receive Data	BB	3	(Data from MODEM)
Request To Send	CA	4	
Clear To Send	CB	5	
Data Terminal Ready	CD	20	
Data Carrier Detect	CF	8	
Transmit Clock	DB	15	(Clock From MODEM)
Receive Clock	DD	17	(Clock From MODEM)
RS-422			
Receive Data	RD-A'	11	
	RD-B'	23	
Receive Timing	RT-A'	9	
	RT-B'	21	
Send Data	SD-A	13	
	SD-B	25	
Terminal Timing	TT-A	12	
	TT-B	24	

In a 5000IS, the first 861 has connector J3 connected to connector J4 on the 971 processor board and J2 on the 861 is connected to channel 2 on the I/O panel. Any additional 861 boards are connected in the following manner:

<u>Board</u>	<u>I1</u>	<u>I2</u>
Second 861	Ch. 3	Ch. 4
Third 861	Ch. 5	Ch. 6
Fourth 861	Ch. 7	Ch. 8

In a 5000SX system, the 861 boards have the following connections to the I/O panel:

<u>Board</u>	<u>I1</u>	<u>I2</u>
First 861	Ch. 3	Ch. 4
Second 861	Ch. 5	Ch. 6
Third 861	Ch. 7	Ch. 8
Fourth 861	Ch. 9	Ch. 10
Fifth 861	Ch. 11	Ch. 12
Sixth 861	Ch. 13	Ch. 14
Seventh 861	Ch. 15	Ch. 16
Eighth 861	Ch. 17	Ch. 18

The odd numbered channels are usually used for terminals and the even numbered channels are used for printers.

MODEL 861 MULTIPROCESSOR BOARD

Legend

- JA Port A Clock Selection (Normally 1-16, 3-14 and 6-11 are shunted.)
- JB Port B Clock Selection (Normally 1-4 are shunted.)
- JD Reset Disable (Normally unshunted.)
- JE I/O Address Selection
- JF Interrupt Level Selection
- J1 Serial Port 0
- J2 Serial Port 1

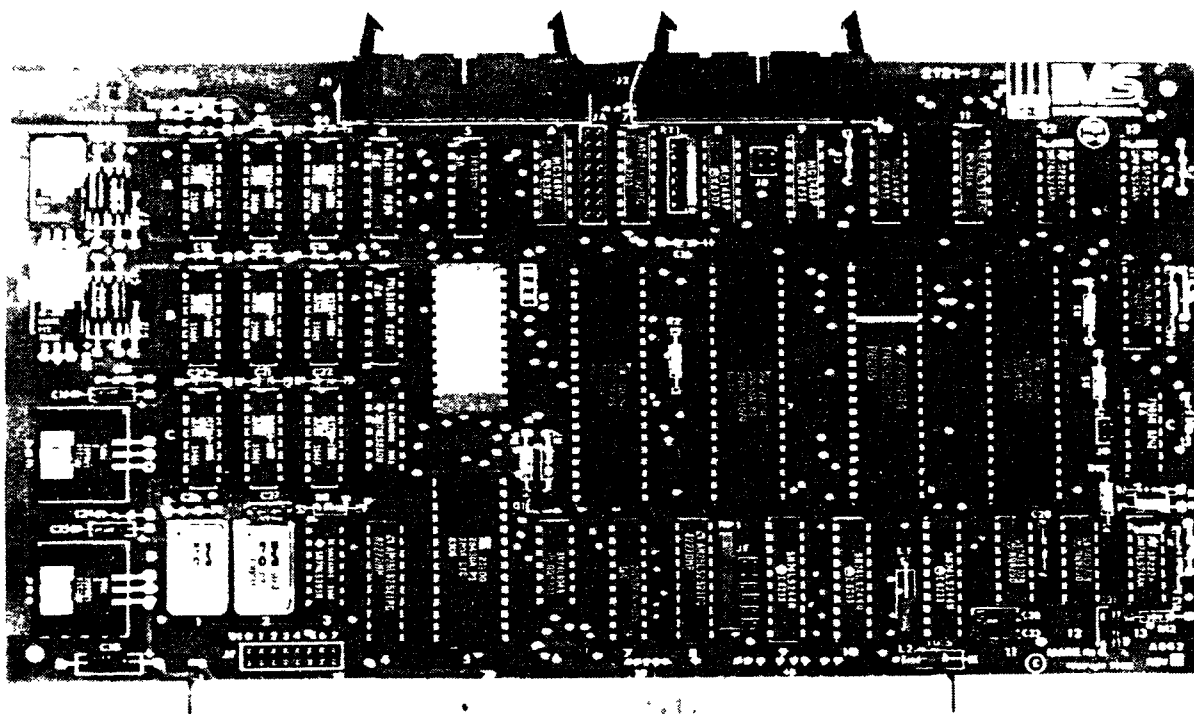


Figure 2-26
Model 861 Multiprocessor Board

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;
; sticky label says "SLVBT REV 1.0 9B49 1/18/83"
;
0000 F3      DI
0001 015A00  LD    BC,90      ;copy myself into R/W memory?
0004 110000  LD    DE,0
0007 210000  LD    HL,0
000A EDB0      LDIR
000C 310009  LD    SP,900H
000F 3ECF      LD    A,0CFH
0011 D326      OUT   (26H),A    ;PIO A cntl
0013 3EFF      LD    A,0FFH
0015 D326      OUT   (26H),A    ;PIO A cntl
0017 3EB0      LD    A,0B0H
0019 D325      OUT   (25H),A    ;PIO B data
001B 3E0F      LD    A,0FH
001D D327      OUT   (27H),A    ;PIO B cntl
001F DB20      IN    A,(20H)    ;??
0021 210009  LD    HL,900H
0024 110400  LD    DE,4
0027 CD4600  CALL   46H
002A 2A0009  LD    HL,(900H)
002D ED5B0209 LD    DE,(902H)
0031 E5      PUSH  HL
0032 CD4600  CALL   46H
0035 E5      PUSH  HL
0036 EB      EX    DE,HL
0037 214000  LD    HL,40H
003A 010600  LD    BC,6H
003D EDB0      LDIR
003F C9      RET

0040 F3      DI
0041 3EB0      LD    A,0B0H
0043 D325      OUT   (25H),A    ;PIO B data
0045 C9      RET

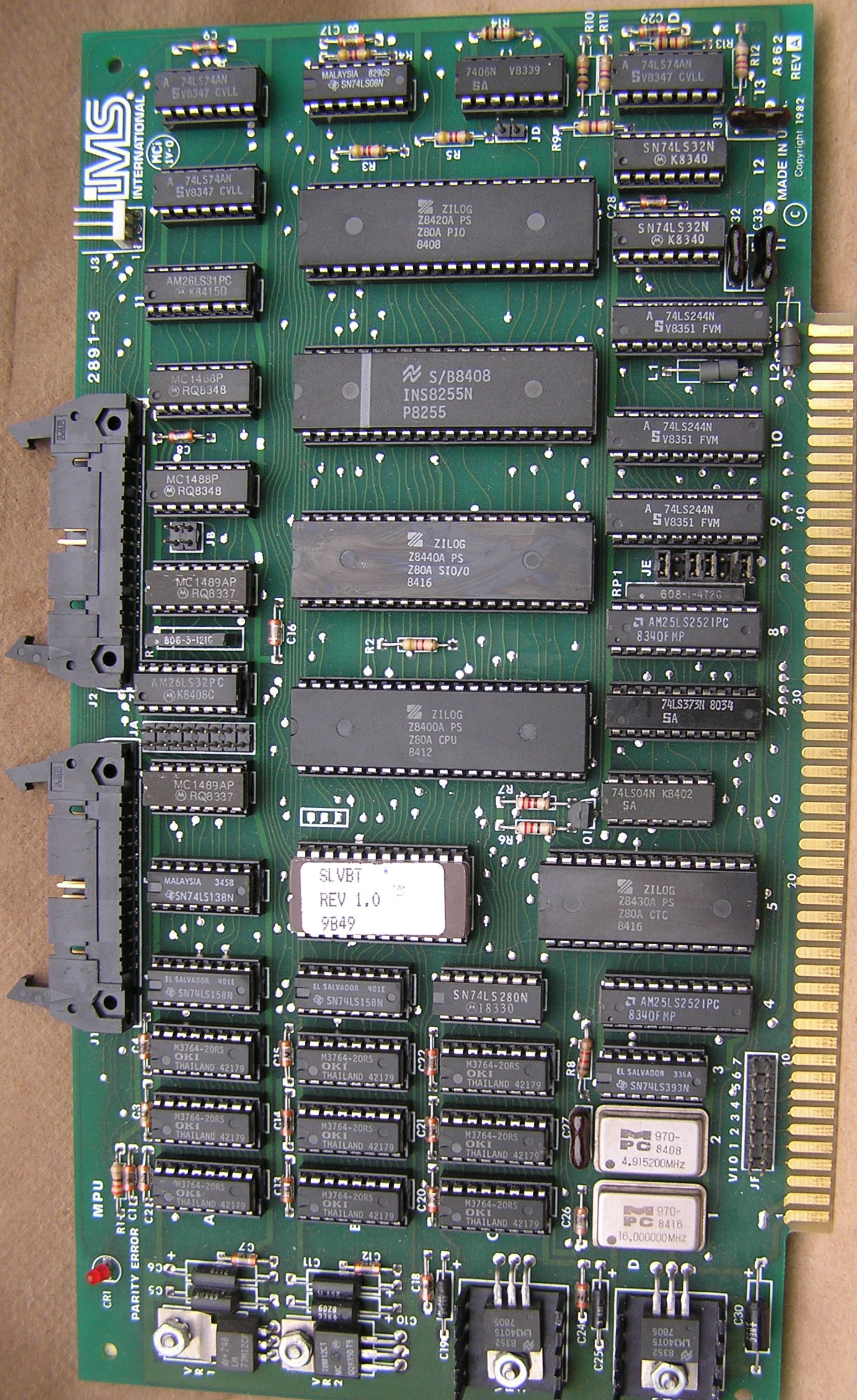
0046 CD5100  CALL   51H
0049 77      LD    (HL),A
004A 23      INC   HL
004B 1B      DEC   DE
004C 7A      LD    A,D

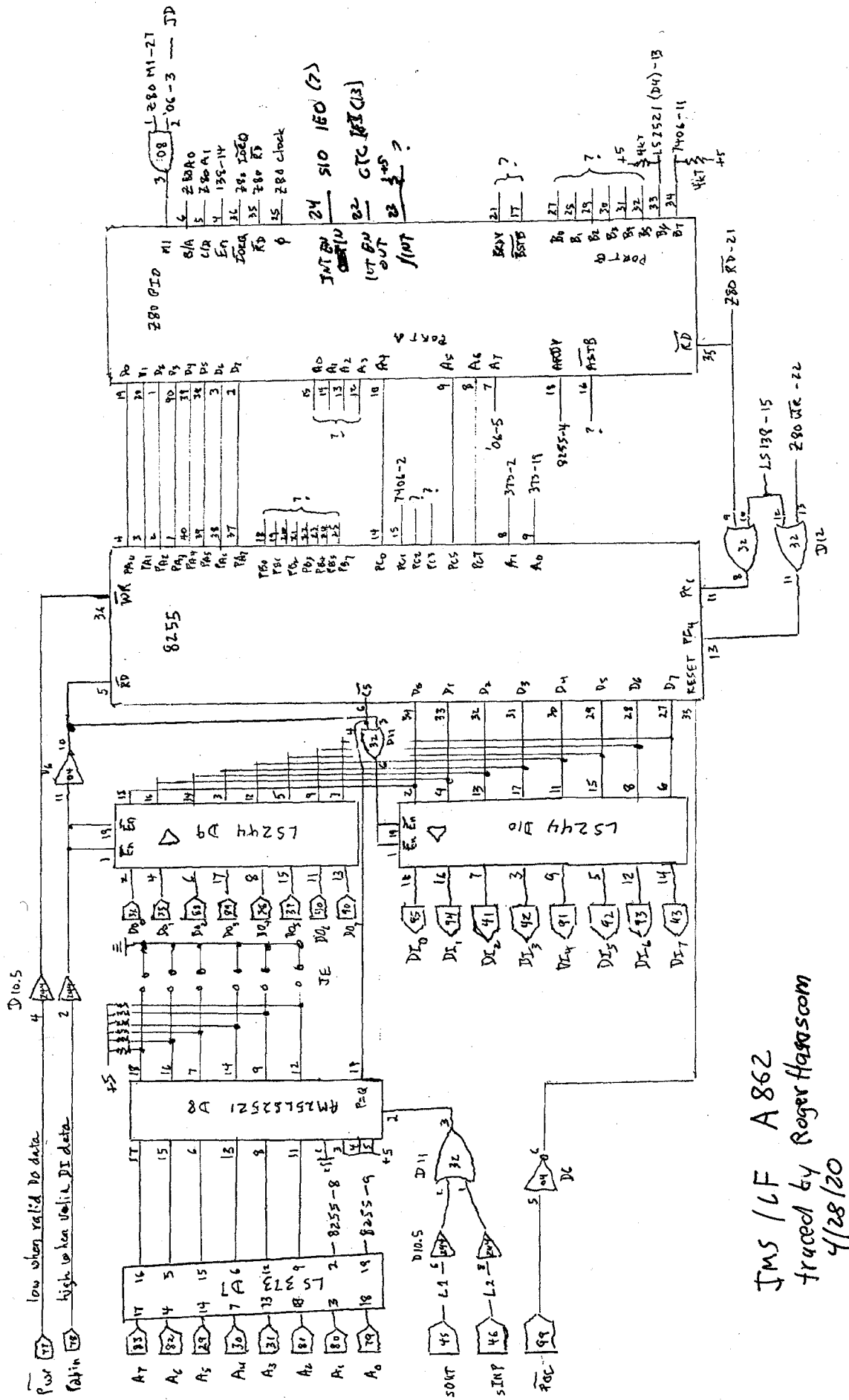
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004D B3      OR    E
004E 20F6          JR    NZ,46H
0050 C9      RET

0051 DB24          IN    A,(24H)      ;PIO A data
0053 CB77          BIT    6,A
0055 20FA          JR    NZ,51H
0057 DB20          IN    A,(20H)      ;??
0059 C9      RET
      ;rest of 2716 is 0FFH

      END
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JMS / LF A862
 traced by Roger Hagascom
 4/28/20